PAPER Special Section on Analog Circuit Techniques and Related Topics

Design and Experiments of a Novel Low-Ripple Cockcroft-Walton AC-to-DC Converter for a Coil-Coupled Passive RFID Tag

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SUMMARY A low-ripple diode charge-pump type AC-DC converter based on the Cockcroft-Walton diode multiplier is proposed for coil-coupled passive IC tags in this paper. This circuit is developed as a power supply for passive RFID tags with smart functions such as heart rate detection and/or body temperature measurement. The proposed circuit converts wirelessly induced power to a low-ripple DC voltage suitable for a 13.56 MHz RFID tag. The proposed circuit topology and the principle of operation are explained and treated theoretically by using quasi-equivalent small-signal models. The proposed circuit was implemented on a PCB. And it was confirmed that the proposed circuit provides 3.3 V DC with a ripple of less than 20 mV when a $4V_{p-p}$ sinusoidal input is applied. Under this condition, the maximum output power is about 310 μW. The measured results were in good agreement with theoretical and HSPICE simulation results.

key words: *RFID, wireless power feeding, AC-DC converter, diode charge pump*

1. Introduction

A half-wave rectifier or a full-wave rectifier is commonly used for an AC-DC converter in a passive RFID tag [1], [2]. However, due to their low power conversion efficiency (PCE), the above circuits are not efficient for low power conversion.

As other AC-DC power conversion circuits for an RFID tag, the Cockcroft-Walton type diode charge pump [3] has been used. These AC-DC conversion circuits have an output ripple V_R given by (1) [4].

$$V_R = \frac{V_{out}}{f_{in} R_L C_{out}} \tag{1}$$

Here f_{in} is the frequency of the input signal. R_L and C_{out} are the load resistance and capacitance, respectively. This ripple should be small in analog signal processing of an RFID tag with smart functions such as heartbeat detection and/or body temperature measurement [5], [6]. The ripple must be less than $0.6\,V_{p-p}@V_{DD} = 3$ V for a heartbeat detection circuit in the present design [5].

Though the on-chip full-wave active rectifier was developed [7] to achieve high PCE, the ripple is not reduced as compared with the conventional full-wave rectifier.

One method to reduce ripple is to use a higher input frequency f_{in}. However, in an RFID application, the available frequency range is fixed by the regulations on wireless communication. The other method to reduce ripple is to use large output capacitance C_{out}. This is not permitted by the limited volume of an RFID tag.

Recently, an automatic current control scheme was developed to reduce ripples [8]. This scheme controls the current flowing into the charge pump circuit by monitoring ripples. However, this circuit cannot operate at frequencies higher than 600 kHz [8] because of its feedback control scheme.

Though a voltage regulator can reduce the output ripple, the regulator cannot operate at high frequencies in the RF band. Hence, in RFID applications, the output ripple must be reduced by the rectifier itself.

To achieve ripple reduction at high frequencies such as tens of megahertz, a symmetrical structure of Dickson-based charge pump was developed [9]. This voltage tripler is designed to reprogram/erase the EEPROMs, so that the output impedance is high and the PCE is low. Additionally, this method requires 8 stages to reduce the ripple by 20% and this circuit occupies large chip area (565 μm × 825 μm).

In this paper, a low-ripple Cockcroft-Walton type diode-charge-pump AC-DC converter for 13.56 MHz passive RFID tags is proposed. This power supply has a high PCE suitable for an application to a passive RFID tag with smart functions (a smart RFID tag [5]). The proposed circuit has very low ripple by adopting a push-pull scheme suitable for a coil-coupled reader-transponder system.

Section 2 describes circuit configuration, analysis by instantaneous equivalent circuits, and HSPICE simulation results. Here, the proposed circuit topology and the principle of operation are explained and treated theoretically. HSPICE simulations were performed with the BAT15-099 Schottky diode device parameters provided by Infineon Technologies [10]. The theoretical results are confirmed to be consistent with the simulation results.

Section 3 describes the implementation of the proposed circuit onto a PCB and the experimental results of the proposed circuit. The operation and performance of the proposed circuit were confirmed with experiments. The measured results are compared with the theoretical and the simulated results.

In Sect. 4, comparison with other works is described to feature the proposed circuit. The fabrication on CMOS process is also discussed.

Section 5 summarizes the conclusions.

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2. Low-Ripple Charge-Pump Type AC-DC Converter

2.1 Circuit Configuration

Figure 1 shows the proposed AC-DC converter which consists of a miniaturized secondary coil and a Cockcroft-Walton diode charge-pump AC-DC converter.

The proposed circuit is constructed by connecting two Cockcroft-Walton multiplier in parallel, with the input signals which have opposite polarities.

In order to reduce the power consumption and to achieve high power conversion efficiency in the frequency range of tens of megahertz, the Infineon BAT15-099 Schottky diodes are used. Its device parameters will be shown later in the section of HSPICE simulations.

Figure 2 shows the equivalent circuit of the proposed circuit. In Fig. 2, L_s, R_{hf}, C_p, and R_{leak} (which consist of an equivalent circuit for a secondary coil) denote the series inductance, the series resistance, the parasitic capacitance, and the leak resistance of the secondary coil, respectively. V_m denotes an induced electromotive force which is generated by electromagnetic coupling with a solenoid primary coil. C_L and R_L denote the load capacitance and load resistance, respectively.

Figures 3 and 4 show how the upper-half of the circuit in Fig. 1 works when V_x takes a negative and a positive value, respectively. The output voltage V_{out} (= V_{C3} = $2(V_{xm} - V_D)$) can be obtained as shown in Fig. 5. Here, V_{xm} is the amplitude of V_x and V_D is diode's forward ON voltage. The ripple voltage in V_{out} mainly arises from discharge currents to the load. In order to reduce this ripple, the charge pumps are connected in parallel with the input signals having opposite polarities as shown in Fig. 2.

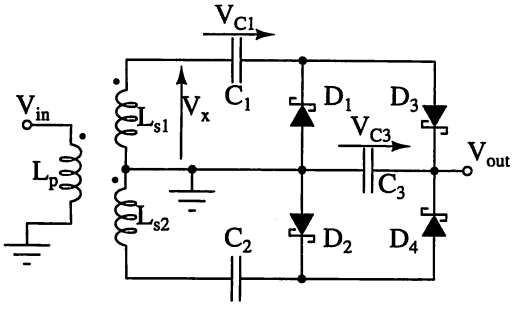

Fig. 1 Proposed circuit.

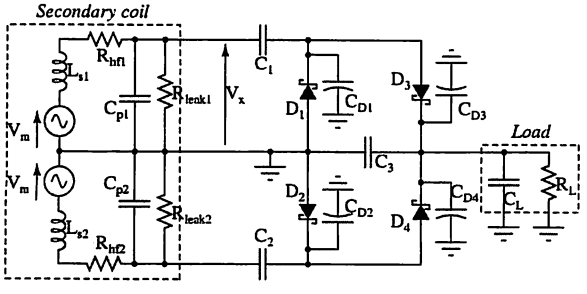

Fig. 2 Equivalent circuit of the circuit in Fig. 1.

2.2 Analysis by Using Instantaneous Equivalent Circuits

In the following, a theoretical design formula for the approximate behavior of the AC-DC converter will be derived assuming that this circuit is in the steady state. Let us first consider a case where only the upper-half portion of the charge pump circuit in Fig. 1 exists. C_{D1}-C_{D4} denote parasitic capacitances to the ground of the diodes D_1-D_4, respectively, which are the well-to-bulk capacitances in case of integration by a CMOS process. The anode-to-cathode parasitic capacitance of a Schottky diode is neglected since a Schottky diode is a majority carrier device and its anode-to-cathode capacitance is small as compared to C_1-C_3.

A theoretical treatment will be done only for the circuit section just after the coil (namely, excepting for the circuit surrounded by the broken line in Fig. 2). An instantaneous equivalent circuit for this AC-DC converter when V_x takes the maximum value (=V_{xm}) is given in Fig. 6. C_T in Fig. 6 is defined by

$$C_T \triangleq C_3 + C_{D3} + C_L \tag{2}$$

ΔQ and ΔQ_{D1} in Fig. 6 denote incremental charges which

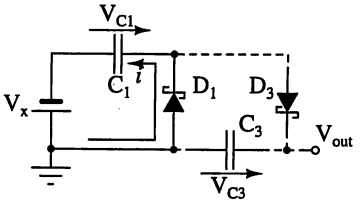

Fig. 3 Upper-half portion of Fig. 1 when V_x takes a negative value.

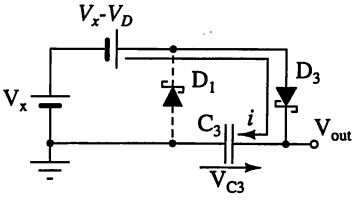

Fig. 4 Upper-half portion of Fig. 1 when V_x takes a positive value.

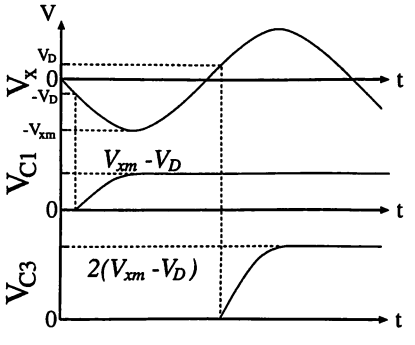

Fig. 5 Theoretical waveform of V_x, V_{C1}, and V_{C3} (R_L: not connected, the initial charges on C_1 and C_3: 0).

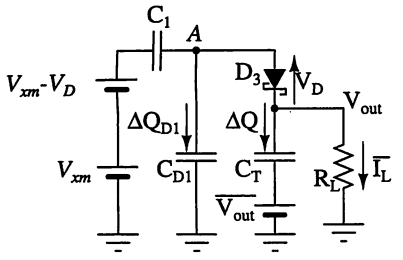

Fig. 6 Instantaneous equivalent circuit when V_x takes the positive maximum value.

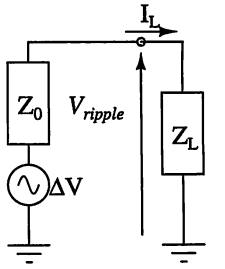

Fig. 7 Quasi-equivalent small-signal model of the circuit in Fig. 6.

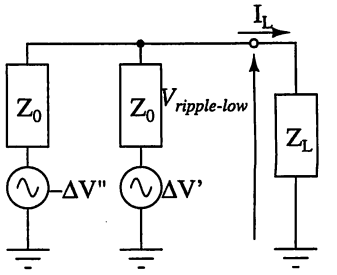

Fig. 8 Quasi-equivalent small-signal model for the proposed low-ripple AC-DC converter.

flow onto C_T and C_{D1}, respectively, during the period where D_1 is OFF and D_3 is ON. V_D in Fig. 6 denotes the on-voltage of each diode. If D_{on} and D_{off} denote the on-state and the off-state duty cycle of the diode D_3. Then, D_{on} and D_{off} satisfy

$$D_{on} + D_{off} = 1 \tag{3}$$

HSPICE simulations showed that the current of D_3 takes an approximately triangular waveform and the duration of the on-state is much smaller than that of the off-state in D_3 if the change of V_{out} due to the load current is small. Then, by assuming the steady state, we obtain the following equation by applying Kirchhoff's voltage law to the circuit in Fig. 6.

$$2V_x - V_D = \frac{1}{C_1}\left(2\Delta Q + \Delta Q_{D1} + \overline{I_L} D_{on} T\right) + V_D + \frac{\Delta Q}{C_T} + \overline{V_{out}} \tag{4}$$

Here, T denotes $T = 2\pi/\omega = 1/f$ where ω is the frequency of the AC voltage induced in a secondary coil by electromagnetic induction. In the above equation, $\overline{V_{out}}$ and $\overline{I_L}$ are the average output voltage and the average output current in Fig. 6, respectively. These are related as

$$\overline{I_L} = \frac{\overline{V_{out}}}{R_L} \tag{5}$$

where R_L is the load resistance in Fig. 6. In addition, as the state of diode D_3 changes from OFF to ON, the node potential of node A in Fig. 6 changes from $-V_D$ to $\overline{V_{out}} + \frac{\Delta Q}{C_T} + V_D$. Therefore, charge ΔQ_{D1} stored in C_{D1} is expressed as follows.

$$\Delta Q_{D1} = C_{D1}\left[\left(\overline{V_{out}} + \frac{\Delta Q}{C_T} + V_D\right) - (-V_D)\right] \tag{6}$$

Furthermore, $\overline{I_L}$ and ΔQ are related as

$$2\Delta Q = D_{off} T \overline{I_L} \tag{7}$$

From the above equations, we obtain

$$\overline{V_{out}} = \frac{2V_x - 2V_D\left(1 + \frac{C_{D1}}{C_1}\right)}{1 + \frac{C_{D1}}{C_1} + \frac{1}{2C_1 R_L f}\left(2 + D_{off}\frac{C_1 + C_{D1}}{C_T}\right)} \tag{8}$$

Figure 7 shows a conceptual quasi-equivalent small-signal model of the circuit in Fig. 6. In this figure, Z_0 is the equivalent output impedance of the upper (or lower) charge-pump circuit and ΔV is the open-circuit output ripple voltage seen across the output port. Z_L is the equivalent load impedance. These quantities are meaningful only in the sense of quasi-equivalent approximation. Then, we obtain

$$V_{ripple} = \frac{\Delta V}{1 + \frac{Z_0}{Z_L}} \tag{9}$$

where V_{ripple} denotes the output ripple. In the same manner, we can obtain a similar equation for a conceptual quasi-equivalent macro-model in Fig. 8 in which $\Delta V'$ and $\Delta V''$ represent the open-circuit output ripple voltages of the upper and lower charge-pump circuits, respectively, of the low-ripple AC-DC converter shown in Fig. 1. For the circuit in Fig. 8, we obtain

$$V_{ripple-low} = \frac{\frac{\Delta V' - \Delta V''}{2}}{1 + \frac{Z_0}{2Z_L}} \tag{10}$$

where $V_{ripple-low}$ is the output ripple of the low-ripple AC-DC converter.

Comparing (9) and (10), we can see that the ripple can be removed if the ripple components of the upper and lower charge-pump circuits of the low-ripple AC-DC converter cancel each other (namely, $\Delta V' = \Delta V''$). Under this condition, the output voltage of the low-ripple AC-DC converter is given by

$$\overline{V_{out-low}} = \frac{2V_x - 2V_D\left(1 + \frac{C_{D1}}{C_1}\right)}{1 + \frac{C_{D1}}{C_1} + \frac{1}{4C_1 R_L f}\left(2 + D_{off}\frac{C_1 + C_{D1}}{C_T'}\right)} \tag{11}$$

where

Table 1 Element values used in the simulations.

C_1, C_2	22 pF
C_3	68 pF
R_{hf1}, R_{hf2}	470 mΩ
R_{leak1}, R_{leak2}	528 Ω
C_{p1}, C_{p2}	300 fF

Table 2 Device parameters of the BAT15-099.

Forward ON voltage V_D	0.224 V
Breakdown voltage V_B	4.2 V
ON resistance R_{ON}	5 Ω
OFF resistance R_{OFF}	15 MΩ
Junction capacitance C_j	138.5 fF
Available frequency	12 GHz

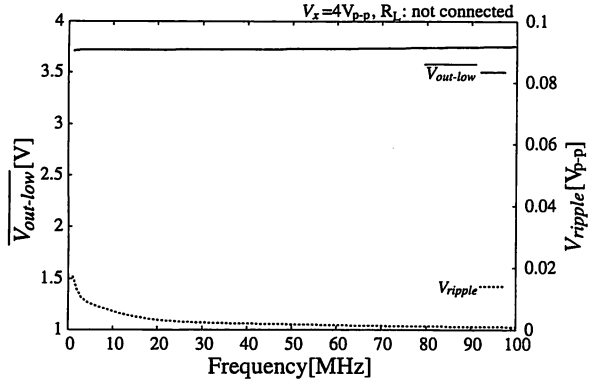

Fig. 9 $\overline{V_{out-low}}$ and V_{ripple} vs. input frequency.

$$C_T' \triangleq C_3 + C_{D3} + \frac{C_L}{2} \tag{12}$$

and the output power is given by

$$P_{out} = \overline{V_{out-low}}\,\overline{I_L} = \frac{\overline{V_{out-low}}^2}{R_L} \tag{13}$$

2.3 Circuit Simulations by HSPICE

The performances of the proposed circuit were confirmed by HSPICE simulations using the BAT15-099 diode model provided by Infineon Technologies AG [10]. The element values and the device parameters of the BAT15-099 are shown in Table 1 and Table 2, respectively.

Figure 9 shows the mean value of the output voltage $\overline{V_{out-low}}$ and the peak-to-peak ripple voltage V_{ripple} when the frequency of the input sinusoidal signal V_x was changed from 1 MHz to 100 MHz with its swing of 4V$_{p-p}$.

Figure 10 shows $\overline{V_{out}}$ and V_{ripple} versus V_x at 13.56 MHz. Since the Schottky-diode breakdown voltage V_B is 4.2 V and the forward ON voltage V_D is 0.2 V, $\overline{V_{out-low}}$ saturates about 4.0 V.

Here, the voltage fluctuation on C_3 (i.e. the output ripple) is generated by the relatively large Schottky diode leakage current and by the load current. In order to observe the ripple generated by the diode leakages, simulations for no load were carried out in Figs. 9 and 10.

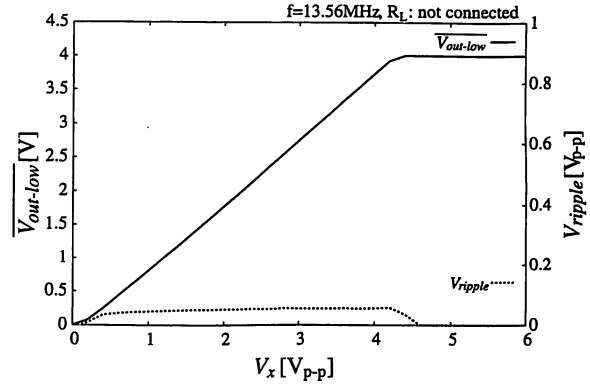

Fig. 10 $\overline{V_{out-low}}$ and V_{ripple} vs. V_x.

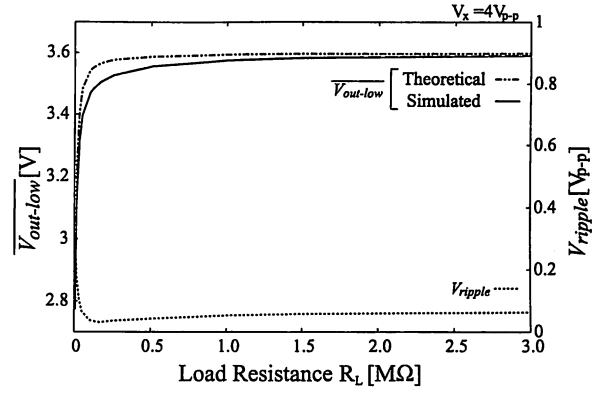

Fig. 11 $\overline{V_{out-low}}$ and V_{ripple} vs. loaded resistance R_L.

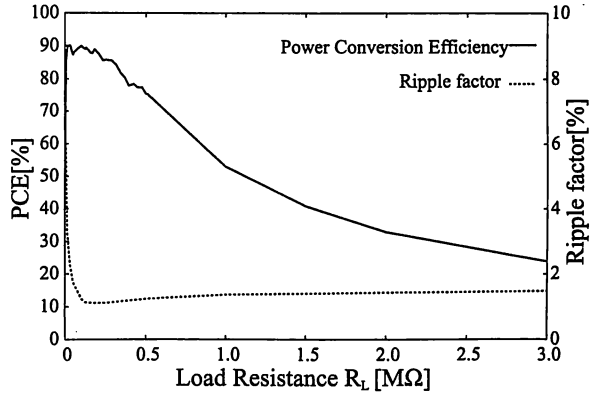

Fig. 12 The PCE and the ripple factor vs. loaded resistance R_L.

In Fig. 11, the theory and simulation are compared regarding $\overline{V_{out-low}}$ and V_{ripple} for when the load resistance R_L is changed.

The output voltage becomes almost independent of the load for $R_L \geq 500\,k\Omega$.

The theoretical value of $\overline{V_{out-low}}$ in Fig. 11 is calculated from (11) assuming $C_1 = C_2$, $C_{D1} \simeq C_{D2}$, $C_{D1} \ll C_1$, $C_1 \ll C_T'$, and $D_{off} \simeq 1$. As shown in Fig. 11, a good agreement is obtained between the simulated and theoretical values of $\overline{V_{out-low}}$ with the precision of better than 5.7%.

Figure 12 shows the power conversion efficiency (PCE)

and the ripple factor under the change of the load. Here, the PCE is defined by the output power divided by the input power, and the ripple factor is defined by V_{ripple} divided by $\overline{V_{out-low}}$. The maximum PCE is 90.2%. The maximum output power is 367 μW when the ripple factor is less than 2.3%.

3. Circuit Implementation on a Printed Circuit Board

3.1 Component Layout

It is difficult to realize stable and well-matched Schottky diodes in the presently available CMOS process because a Schottky diode requires very thin oxide layer between metal and semiconductor. Therefore the element values of the Schottky diodes widely deviate in the typical CMOS process. However, the ripple reduction in the proposed circuit based on canceling of ripples with 180° phase difference, so that the poorly matched diodes degrade the ripple reduction capability. In order that the proposed ripple-reduction technique may work well, the proposed circuit must be fabricated by using well-matched diodes.

From above reasons, the proposed circuit in Fig. 1 (excepting coils; see Fig. 13) was fabricated on a printed circuit board (PCB) with BAT15-099 Schottky diodes and chip capacitors. A BAT15-099 contains 2 Schottky diodes as shown in Fig. 13.

A photograph of the fabricated PCB is shown in Fig. 14. This PCB consists of four layers, and the one of the layers is filled with metal which is used as the GND layer.

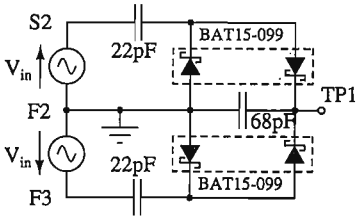

Fig. 13 Circuit layout fabricated on a PCB.

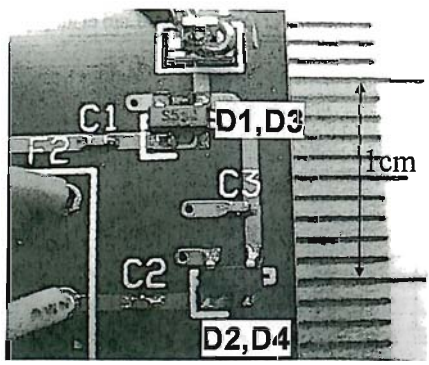

Fig. 14 A photograph of the proposed AC-DC converter fabricated on a PCB.

3.2 Experimental Results

In the experiments, the input voltage was generated by the arbitrary waveform generator YOKOGAWA AG4100. The digital oscilloscope AG4100 was used to measure the voltages.

Figure 15 shows $\overline{V_{out-low}}$ and the peak-to-peak ripple voltage V_{ripple} under unloaded condition and 1 MΩ loading when the input is swept from 1 MHz to 80 MHz with its swing of 4 V_{p-p}.

The lack of data in Fig. 15 around 55–70 MHz is due to that the arbitrary waveform generator cannot generate 4 V_{p-p} input voltage by the resonance of the PCB. This problem will be alleviated by adopting special GND layer preventing eddy currents. As shown in Fig. 16 (upper trace: V_{in}, lower trace: V_{out}), the circuit in Fig. 13 converts AC 4V_{p-p} to DC 3.4 V without ripple at the frequency of 13.56 MHz. At frequency higher than 50 MHz, the peak-to-peak ripple voltage becomes appreciably large. Since the ripple frequency is the input frequency, it may be caused by the leak of the input signal via the GND layer. This will be reduced by reducing the parasitic capacitance between the GND layer and the input node.

The $\overline{V_{out-low}}$ and the V_{ripple} for the load from 7.5 kΩ to 1MΩ are shown in Fig. 17.

When the load is less than 15 kΩ, the ripple becomes

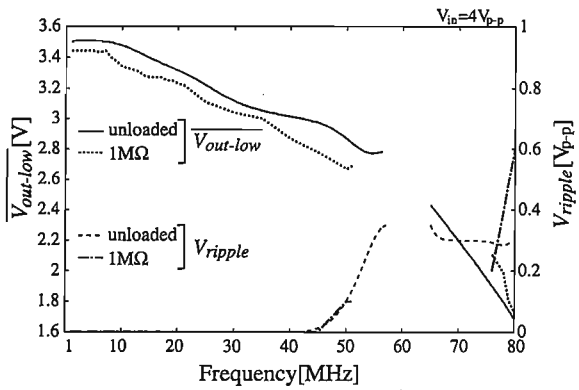

Fig. 15 Measured $\overline{V_{out-low}}$ and V_{ripple} of the PCB in Fig. 13 vs. input frequency.

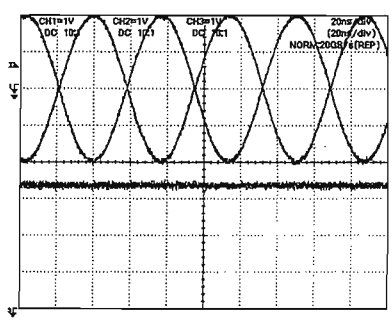

Fig. 16 Traces of V_m's and V_{out} on the oscilloscope display (unloaded, V_{in}: 4V_{p-p}@13.56 MHz).

appreciably large as shown in the lower trace of Fig. 18. The second harmonic component of the input frequency was observed as a residual ripple in the output. This is generated by imperfect ripple cancellation due to asymmetrical waveforms of the ripple. The rise time of the ripple depends on the ON resistance of the diodes and the fall time of the ripple depends on the load resistance. Therefore, the ripple increases as R_L decreases.

The maximum output power was about 310 μW when the ripple factor was less than 1.1%, R_L = 30 kΩ, $\overline{V_{out-low}}$ = 3.05 V (namely, load current≃ 100 μA).

For a load greater than or equal to 510 kΩ, this circuit can output 3.3 V DC with a very small ripple.

At $V_{in} = 4V_{p-p}$@13.56 MHz and R_L = 30 kΩ, the theoretical (calculated from (11)), simulated, and measured values of $\overline{V_{out-low}}$ are 3.41 V, 3.32 V, and 3.05 V, respectively.

As shown in lower trace of Fig. 19, V_{ripple} was reduced to 20 mV_{p-p}. Notice here that the lower trace in Fig. 19 is shown with the range of 10 mV/div.

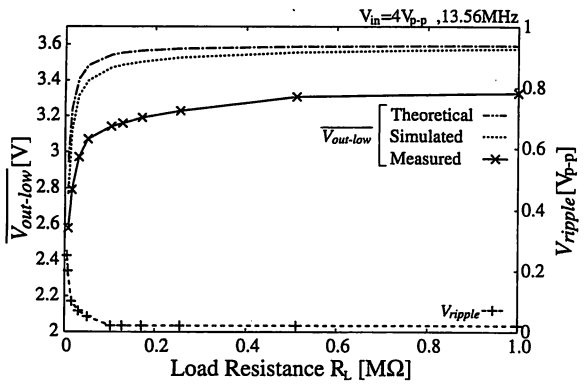

Fig. 17 Measured $\overline{V_{out-low}}$ and V_{ripple} vs. resistive load.

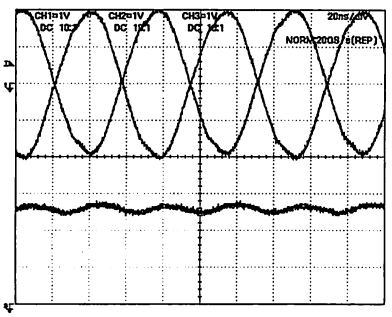

Fig. 18 Traces of V_{in}'s and V_{out} on the oscilloscope display (R_L=7.5 kΩ, V_{in}: $4V_{p-p}$@13.56 MHz).

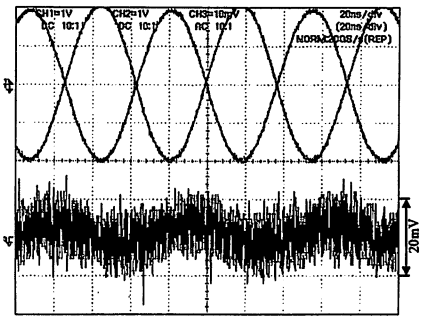

Fig. 19 Traces of V_{in}'s and V_{out} on the oscilloscope display (R_L=1 MΩ, V_{in}: $4V_{p-p}$@13.56 MHz).

4. Discussions

Table 3 shows comparison between the proposed circuit and the other comparable works. The AC-DC converter of [8] is designed for USB-OTG (On-The-Go) application which needs high power and low ripple. In order to achieve high output power, an off-chip large output capacitor (330 nF) is used. Since an automatic pumping control scheme is used to obtain good ripple reduction, the number of MOSFETs used is relatively large (i.e., the PCE degrades to 70%) and the operation frequency is low.

The AC-DC converter of [9] is designed for rewriting EEPROM. Good ripple reduction is obtained by using 8-stage asymmetrical structure. This structure is similar to the ripple reduction scheme of the proposed circuit in concept. However, since the circuit uses many MOSFETs which operates in saturation region, dissipated power is relatively large (i.e., PCE is low).

On the other hand, the circuits of [7] and [11] are de-

Table 3 Comparison with other AC-DC converters.

Property	This work	Kim et al. [8]	Bedeschi et al. [9]	Balachandran et al. [11]	Lam et al. [7]
Core rectifier	Cockcroft-Walton multiplier	Dickson charge pump	Dickson charge pump	Cockcroft-Walton multiplier	original (full-wave rectifier based)
Implementation	on-board	on-chip	on-chip	on-chip	on-chip
Dissipative elements	4 Schottky diodes	more than 40 MOSFETs	96 MOSFETs + 24 inverters	12 Schottky diodes	40 MOSFETs
PCE	90%	70%	NA †	NA	87%
Ripple factor	1.1%	0.75%	0.30%	13.6%	9.3%
V_{ripple}	<20 mV_{p-p}	≤33.8 mV_{p-p}	≤16 mV_{p-p}	<0.3V_{p-p}	<0.3V_{p-p}
Frequency	1–50 MHz ††	400–600 kHz	15.6 MHz	900 MHz	13.56 MHz
Input amplitude	2 V	3.3 V	1.8 V	1.8 V	3.5 V
$\overline{V_{out}}$	3.4 V	4.5 V	5.5 V	2.2 V	3.2 V
Max. output power (Output capacitor)	310 μW (68 pF)	135 mW (330 nF)	1.99 mW (200 pF)	110 μW (250 pF)	5.76 mW (200 pF)

† NA: not available †† Target frequency is 13.56 MHz

signed as a power supply for RFID tags. The AC-DC conversion ripple V_{ripple} is not reduced so far from that of a full-wave rectifier in those AC-DC converters, so that these circuit will not be suitable for a power supply for a smart RFID tag with biomedical signal processing functions.

As shown in Table 3, the advantages of our work are higher PCE, smaller number of elements, good ripple reduction. Additionally, higher output power can be obtained by using a larger C_1 at the cost of increased volume. Though the circuit scale becomes larger by the on-board implementation, it can be implemented within the size of 3 mm × 12 mm. This size meets the present specification for a passive smart RFID tag. The off-chip realization is favorable in the respect that the AC-DC converter for a smart RFID tag must provide more than several hundreds of milliwatts.

By using the diode-connected MOSFETs [7], [9] or by using controlled MOSFET switches in stead of using Schottky diodes, a fully CMOS version of the proposed circuit can be fabricated by a 0.35 μm/0.25 μm CMOS process and will supply the output power of less than milliwatts at 13.56 MHz with on-chip capacitors.

5. Concluding Remarks

A low-ripple low-power Cockcroft-Walton AC-DC converter suitable for a passive smart RFID tag has been proposed. Its topology and the principle of operation are explained and treated theoretically. The proposed circuit was implemented on a PCB and its performance was confirmed with experiments. This circuit outputs almost constant 3.3 V DC for a load of greater than 510 kΩ when the input is $4V_{p-p}$. The maximum output power was 310 μW when the output voltage is 3.05 V and the load is 30 kΩ. A good agreement is obtained with the theoretical, simulated, and measured results.

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