別紙様式８

研　究　主　論　文　抄　録

論文題目

Development of Dual Loudspeaker System for Controlling Unidirectional Sound Propagation in Low Frequency Range.

（低周波数帯域における単一指向性音響信号伝搬制御を目的とした２スピーカシステムの開発に関する研究）

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主論文要旨

The system very large scale integration (VLSI) market has become diversified and has experienced frequent standard changes, which require various types of products to be manufactured in low volume. In addition, with the development of high integration density, VLSI designs are becoming more complex and longer design cycles are required. All of these trends require high costs for both development and fabrication. Reconfigurable logic devices such as field-programmable gate arrays (FPGAs) are used widely as a solution to the above problems. FPGAs are pre-fabricated devices that can be electrically programmed to become almost any kind of digital circuit or system.

However, the large quantity of configuration memory bits used for logic, routing and user applications make reconfigurable logics undependable when soft error such as single event upset (SEU) occurs. The SEU is usually caused by particles from the outer space or the chip package and produces bit flipping in memory elements of electronic device, and consequently induces soft errors into the system. Because memories in a reconfigurable logic are not only for user applications, but also determine logic and routing connections, any incorrect value of a configuration memory may lead to unexpected consequences.

In order to solve the above problems, high dependability reconfigurable logic technology is researched in this thesis. An error detect and correct circuit (EDAC) is proposed to protect memories of reconfigurable logics from SEU. However, employing protection circuits commonly degrades performances of the target device. Therefore, a three-dimensional (3D) routing architecture is presented to improve the area and the

delay performances for reconfigurable logics. The design and implementation computer aided design (CAD) flow for the proposed device is also introduced.

This thesis consists of six chapters. Chapter 1 introduces the motivation and objectives.

Chapter 2 introduces common device architectures and techniques that related to this thesis, which include island-style FPGA, dependability issues of reconfigurable logics, three-dimensional (3D) FPGA architectures and common design flows. At last, based on approaches and considerations of related researches, research problem definition and focus of this thesis are given.

Chapter 3 describes an error detect and correct circuit (EDAC), which we proposed to protect SRAM of reconfigurable logic device from soft errors. The EDAC circuit detects errors with hamming code technique, covers errors with backup memory, and then the configuration memory can be repaired without stopping user circuits. According to evaluation results, when compared to conventional triple modular redundancy (TMR) method, the proposed high dependability reconfigurable logic had approximately the same area and delay performance while the dependability was 6.8 to 10 times better.

Chapter 4 proposes a face-to-face stacked two layers 3D FPGA architecture. This 3D FPGA architecture reduces on-board area of an FPGA in half, which improves area and delay overhead of employing dependable modules such as EDAC. Smaller on-board size also decreases the possibility of soft error. The proposed 3D routing architecture is a realistic architecture under present technologies when considering the thermal issue and the through-silicon-via area overhead. Evaluation showed that the proposed 3D FPGA used 48.75% less on-board area and 30.54% less critical path delay than a conventional 2D 4-inputs lookup table island-style FPGA on average.

Chapter 5 introduces a design and implementation flow for reconfigurable logics. By using the proposed routing tool, the EasyRouter, it is possible to implement new 2D or 3D reconfigurable logic architectures efficiently. EasyRouter can also generate a part of hardware description language (HDL) codes automatically to reduce development cost for reconfigurable logics. The proposed flow based on EasyRouter bridges academic FPGA design CAD with commercial VLSI design CADs efficiently. And by using this flow, it is possible to perform high accuracy evaluation for target device with commercial VLSI design CADs.

Finally, contributions of this thesis are concluded in chapter 6. Architectures, techniques and results of each chapter are reviewed together. Based on discussion and analysis, future prospects of this field are described.