37－28　Design and Fabrication of MOS Device Circuits with Reticle-Free Exposure Method

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In fabrication of semiconductor devices, increase in mask cost and mask turn-around-time (TAT) becomes serious problem. Furthermore, it is frequently necessary to change the design for circuit correction and additional function after the mask production. Consequently, development cost becomes high and production period becomes long. On the other hand, the market is diversified by informational globalization. In order to fill it, the product cycle must be in short-period extremely. The semiconductor manufacture industry is demanded to make large-item small- volume products with shorter TAT and lower price. In order to solve these problems, several approaches for maskless lithography have been proposed. Among them liquid crystal display (LCD) in place of the mask for the optical lithography have been demonstrated. In our previous work, the method of exposure with LCD projection image and the algorithm of circuit pattern data conversion have already been reported as reticle-free exposure method. However, actual semiconductor device fabrications by reticle-free exposure method have not been discussed. The purpose of this paper is to verify the reticle-free exposure method being applicable to LSI manufacturing. The design and fabrication results for n-MOS transistor process with reticle-free exposure method shown in order to compare with conventional design and fabrication.

（Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials　2004.9）